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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/647,604	08/25/2003	Peter J. Hopper	NSC1-M3000 (P05657)	2816

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EXAMINER	
MONDT, JOHANNES P	
ART UNIT	**PAPER NUMBER**
3663	

DATE MAILED: 08/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/647,604	HOPPER ET AL.	
	Examiner	Art Unit	
	Johannes P. Mondt	3663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Amendment filed 5/22/06 forms the basis for this office action. Applicants cancelled all previously pending claims 1-8 and submitted new claims 9-16. Comments on Remarks submitted with said Amendment are included below under "Response to Arguments".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. ***Claims 9-11 and 13-16*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yama (6,121,657) in view of Applicant's Prior Art as Admitted in the specification.

On claim 9: Yama teaches a MOSFET structure (see abstract) formed in a substrate 6 of semiconductor material having a first conductivity type (p-type) (col. 3, lines 58-63), the MOSFET structure comprising:

an active region 6 of the substrate (all of region 6 is active; Figures 1B and 1C) having a substantially rectangular perimeter (Figure 1A);

perimeter isolation dielectric material 7 (col. 3, lines 58-67) formed in the substrate (cf. Figs. 1B and 1C; N.B.: any region abutting another region can be viewed to be in said another region);

spaced apart source and drain regions (consisting of source regions 1a and drain regions 1b, respectively, having a second conductivity type (n-type) (col. 3, lines 34-49) opposite said first conductivity type formed in the active region 6 to define a substrate channel region therebetween (region of 6 between 1 a and 1b), both source and drain regions also being spaced apart from the perimeter dielectric isolation material (cf. Figures 1B and 1C); and

a conductive gate electrode 2 (col. 3, line 65 – col. 4, line 35) that consists of two portions:

(a) a first portion that extends over the substrate channel region, i.e., by definition all points of said gate electrode vertically (i.e., normal to the main upper surface of the semiconductor substrate) above any point in the substrate located on a straight line intersecting with at least one source region and one of the drain regions that are said source region's nearest neighbor among all drain regions (first portion indicated in Drawing D appended to this office action) (N.B.: any such point in said substrate is in the substrate channel region because an electric field pointing from drain to source along said straight line exists and ,except for a single isolated saddle point, is non-zero by virtue of the voltage difference between source and drain and hence is in a laterally defined area of said substrate wherein the gate can create a channel for the current; with regard to the saddle point, said first portion extends over said saddle point because it extends over any domain containing said saddle point) and

(b) a second portion that extends continuously over the entire interface between the isolation dielectric material 7 and the active region (cf. Figures 1B and 1C: complement of first portion is a contiguous portion abutting 7) (see Drawing D appended to this office action);

the conductive gate electrode being separated from the substrate channel region by intervening dielectric material (this is inherent in any MOS (=metal-oxide-semiconductor) transistor as disclosed (see abstract), the conductive gate electrode 2 including a first opening 4 formed there through over the source region 1a (Figures 1A and 1B) and a second opening 4 formed there through over the drain region 1b (Figures 1A and 1C).

Yama does not necessarily teach the limitation that the aforementioned perimeter isolation dielectric material is formed along the entire substantially rectangular perimeter of the active region and thus to define a continuous substantially rectangular interface between the isolation dielectric material and the active region. However, it would have been obvious to include said limitation in view of Applicant's Prior Art as Admitted in the specification on page 2, showing perimeter isolation dielectric material 102 (see Prior Art Figures 1A and 1B and page 2, line 8) formed along the entire substantially rectangular perimeter of the active region 110/112/116, thereby defining a continuous, substantially rectangular interface between said isolation dielectric material and said active region.

Motivation to include the teaching by Applicant's Prior Art as Admitted by Applicant stems from the substantially rectangular form of the active region that is to be

protected by said perimeter isolation dielectric material, on account of which it is only a logical consequence of its very purpose as stated by Yama, namely: to enclose the active region (see col. 3, lines 60-64).

On claim 15, said claim 15 merely recites steps in the process of manufacturing the device as claimed. The device of claim 1 would necessarily have to be formed in order to function. Claim 15 fails to further limit the device of claim 9 other than simply form each of their components.

On claim 10: said perimeter isolation dielectric material 7 comprises silicon dioxide (LOCOS = local oxidation of silicon) (col. 3, line 62).

On claim 11: the conductive gate electrode by Yama comprises polysilicon (col. 3, line 35).

On claim 13: the first conductivity type is p-type (col. 3, lines 58-63).

On claims 14 and 16: Applicant's disclosure does not teach why the range as claimed is critical to the invention. Instead, Applicants merely state their "belief" that the range should be what is claimed (see page 8 of the Specification), and even this belief is limited to imager art only while nothing in the claim language limits the invention to this art. In view of the absence of a teaching why a range is critical to the invention Applicant is reminded that it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. With regard to claim 16, said claim merely recites steps in the process of manufacturing the device as claimed. The device

of claim 14 would necessarily have to be formed in order to function. Claim 16 fails to further limit the device of claim 14 other than simply form each of their components.

2. ***Claim 12*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Yama and Applicant's Prior Art as Admitted in the specification as applied to claim 9 above, and further in view of Wolf (ISBN: 0-961672-5-3).

As detailed above, claim 9 is unpatentable over Yama in view of Applicant's Prior Art as Admitted in the specification, neither however teaching the further limitation defined by claim 12.

However, it would have been obvious to include said further limitation in view of Wolf, who, in a text book introduction to MOS transistors, teaches that silicon dioxide is the most common selection for the gate dielectric material in a MOS transistor (see line 4 of 3.1.1 on page 85). Examiner takes official notice that this common and time-honored selection is at least *motivated* due to ease of making, silicon already being in place as an upper portion that merely needs to be oxidized.

Response to Arguments

Applicants' first argument (Remarks, pages 5-6) in traverse is an alleged distinction of the invention as disclosed by Figure 3 and the device by Yama. Applicants specifically allege that

"Yama discloses a MOSFET transistor structure in which the drain includes a multiplicity of source diffusion regions formed in the same active device substrate"

and that

"the gate electrode is one solid piece of conductive material that extends over the entire active region, except for open portions that expose the multiple drain regions and the multiple

source regions so that a conductive interconnect structure be dropped down through vias in the dielectric material to contact the multiple drain regions and multiple source regions",

and that

"this is completely unlike the Figure 3 structure".

However, nothing in the claim language limits said spaced-apart source region and said spaced apart drain region (in the substrate) to be contiguous.

The claims as newly added constitute substantially amended claim language examined for the first time here. The difference between the old claims 1-8 and the new claims 9-16 is that the gate electrode is claimed to consist of one portion extending over the substrate channel and a second portion extending continuously over the entire substantially rectangular interface between the isolation dielectric material 304 and the active region 306.

To meet the new claim limitation the first portion can be defined by definition to be the collection of all points of said gate electrode vertically above (vertically meaning: normal to the main upper surface of the semiconductor substrate) any point in the substrate with a plan view projection located on a straight line intersecting with at least one source region and one of the drain regions that are said source region's nearest neighbors among all drain regions (first portion F indicated in Drawing D appended to this office action) (N.B.: any such point in said substrate is in the substrate channel region because an electric field pointing from drain to source along said straight line exists by virtue of the voltage difference between source and drain and hence is in a laterally defined area of said substrate wherein the gate can create a channel for the

current). The second portion, indicated as S in Drawing D, is defined as the complement of said first portion F, i.e., that portion of said gate electrode not part of said first portion.

Applicants' final argument that "there is nothing in the Yama reference, or the Wolf reference also cited by Examiner, that hints of any appreciation of providing a MOSFET transistor structure that minimizes band-to-band and trap-assisted tunneling mechanism that can lead to gate induced drain leakage characteristics unfortunately does not pertain to any aspect of the present claim language.

For the above reasons the new claims 9-16 are rejected in this office action over the same prior art as was applied for now-cancelled claims 1-8.

Conclusion

Applicant's amendment necessitated the new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

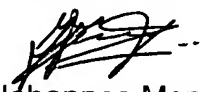
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JPM
August 4, 2006

Patent Examiner:

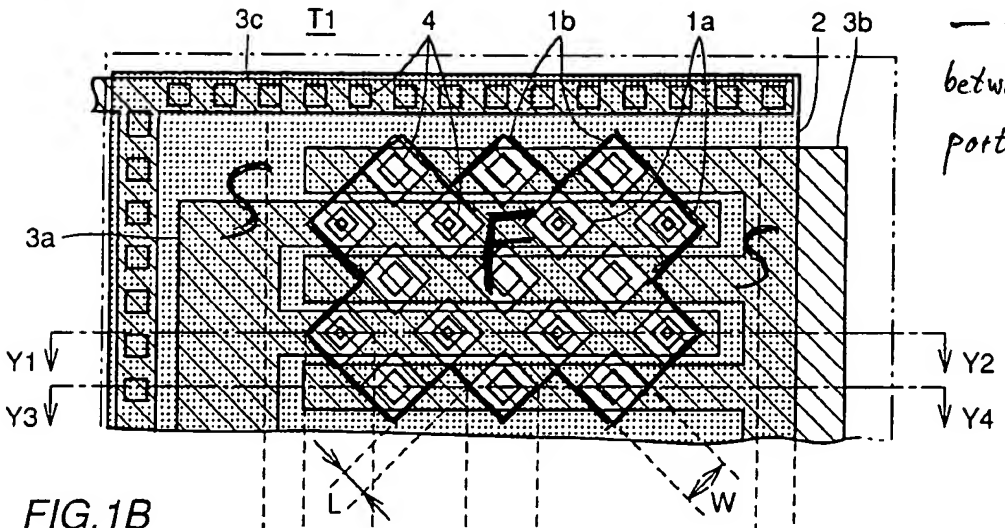


Johannes Mondt (Art Unit: 3663)

Enc: s/a: Appendix to Action (1 page)

APPENDIX TO ACTION 10/647,604

FIG. 1A



— = boundary between first (inner) portion F

FIG. 1B

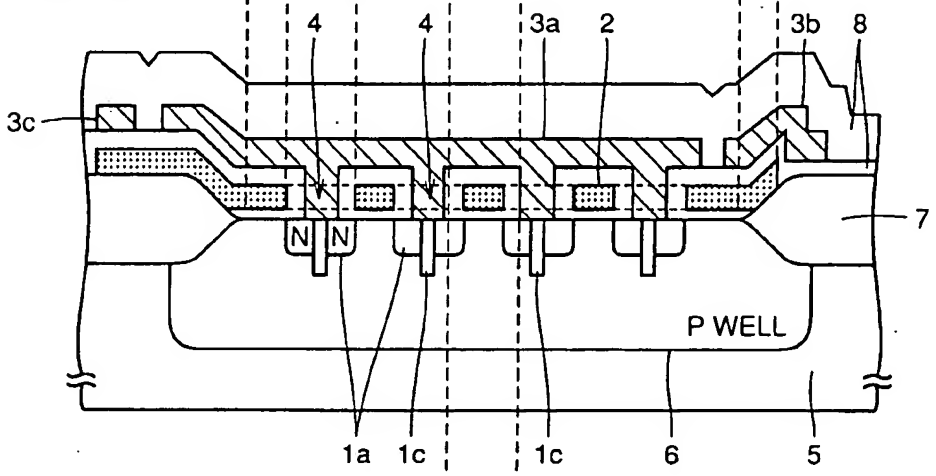


FIG. 1C